

## CLAIMS

We claim:

1. A semiconductor integrated circuit comprising:

a plurality of data output pins;

5 a data processing circuit to generate output signals responsive to an input signal; and

an output selection circuit with at least a normal mode and a test mode;

where a first group of output signals are provided to a first group of data output pins  
in a first test cycle of the test mode; and

where a second group of output signals are provided to a second group of data output  
10 pins during a second test cycle of the test mode.

2. The semiconductor integrated circuit of claim 1 where the output selection  
circuit repeats the first and second test cycles during testing.

15 3. The semiconductor integrated circuit of claim 1

where the output selection circuit sends  $i$ th output signals ( $i$  being a positive integer)  
to  $i$ th data output pins during the first cycle of the test mode; and

where the output selection circuit sends  $(i+1)$ th output signals to  $i$ th output pins during  
the second test cycle of the test mode.

20 4. The semiconductor integrated circuit of claim 1

where the output selection circuit sends  $i$ th output signals ( $i$  being a positive integer)  
to  $(i+1)$ th data output pins during the first cycle of the test mode; and

where the output selection circuit sends the  $(i+1)$ th output signals to  $(i+1)$ th output  
25 pins during the second test cycle of the test mode.

5. The semiconductor integrated circuit of claim 1

where the output selection circuit sends first to  $(N/2)$ th output signals ( $N$  being an  
integer) to first to  $(N/2)$ th data output pins during the first cycle of the test mode; and

30 where the output selection circuit sends  $((N/2)+1)$ th to  $N$ th output signals to first to  
 $(N/2)$ th output pins during a second test cycle of the test mode.

6. The semiconductor integrated circuit of claim 1

where the output selection circuit sends the first to  $(N/2)$ th output signals ( $N$  being a integer) to the  $((N/2)+1)$ th to  $N$ th data output pins during the first cycle of the test mode; and  
where the output selection circuit sends the  $((N/2)+1)$ th to  $N$ th output signals to the  $((N/2)+1)$ th to  $N$ th output pins during the second test cycle of the test mode.

7. A method for outputting data during a test mode of a semiconductor integrated circuit having a plurality of data output pins, the method comprising:  
sending some output signals to a first group of the data output pins; and  
sending remaining output signals to the first group of the data output pins.

8. The method of claim 7 where the sending some output signals and the sending remaining output signals are repeated during a test mode.

9. The method of claim 7 where sending some output signals includes sending  $i$ th output signals ( $i$  being a positive integer) are sent to  $i$ th data output pins.

10. The method of claim 9 where  $i$  is a positive odd integer.

11. The method of claim 7 where sending remaining output signals includes sending  $(i+1)$ th output signals ( $i$  being a positive integer) to  $i$ th data output pins.

12. The method of claim 7 where sending some output signals includes sending first to  $(N/2)$ th output signals ( $N$  being a positive integer) to first to  $N/2$ th data output pins.

13. The method of claim 12 where sending remaining output signals includes sending  $((N/2)+1)$ th to  $N$ th output signals are sent to the first to  $(N/2)$ th data output pins.

14. The method of claim 7 where sending some output signals includes sending first to  $(N/2)$ th output signals ( $N$  being a positive integer) to the  $((N/2)+1)$ th to  $N$ th data output pins.

15. The method of claim 14 where sending remaining output signals includes sending  $((N/2)+1)$ th to  $N$ th output signals to the  $((N/2)+1)$ th to  $N$ th data output pins.